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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/456,230	12/07/1999	MYLES WAKAYAMA	36159/JWE/B600	6158

7590 12/02/2002

Christopher C. Winslade
McAndrews Held & Malloy
500 W. Madison Street
Suite 3400
Chicago, IL 60661

EXAMINER

TRA, ANH QUAN

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/456,230	WAKAYAMA ET AL.
	Examiner Quan Tra	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 August 2002.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 8-11,21 and 22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 8-11,21 and 22 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 4) Interview Summary (PTO-413) Paper No(s) _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/12/2002 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 8-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghoshal (USP 5068628)(previous cited) in view of Hsu (USP 5805003)(previous cited) and Barrett et al. (USP 5243599) (previous cited).

As to claim 8, Ghoshal shows in figure 2 a phase lock loop comprising: a detector (phase detector in circuit 76) for comparing a phase or frequency characteristic of an input signal (26) to a phase or frequency characteristic of a timing reference signal (74); a timing reference signal generator (46, 48,..., 56, 78), connected in feedback fashion to provide a timing reference signal to the detector; a loop filter (FILTER in circuit 76) coupled between the detector and the timing reference generator (inherent), the loop filter developing a control voltage (70) for controlling the operational frequency of the timing reference generator; a frequency divider (N divider 72)

coupled between the timing reference signal and the detector, a phase selected circuit (78) for selecting between among the multiphase signals (58-68). Thus, figure 2 shows all elements of the claim except for the timing reference signal generator is operatively configured to produce an output signal at a characteristic frequency an integral multiple M of a desired output clock frequency. However, Hsu shows in figure 1 a frequency divider circuit (M divider) for reducing the output frequency of a phase lock loop circuit. Therefore, it would have been obvious to one having ordinary skill in the art to add a frequency divider (M divider) to the output of Ghoshal's figure 2 for the purpose of reducing the output frequency, wherein the value of M is selected depending upon particular application. Thus, the reference of Ghoshal's figure 2 and Hsu's figure 1 show all elements of the claim 8 except for the phase select MUX is a Gray code MUX. However, Barrett et al. shows in figure 3 a Gray code MUX with the advantage of providing faster control path than other types of decode devices. Therefore, it would have been obvious to one having ordinary skill in the art to employ the teaching of Barrett et al. in to the Ghoshal's MUX for the purpose of having faster control path.

As to claims 9, Barrett et al.'s figure 3 shows the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

As to claim 10, it is seen as an obvious design choice for selecting frequency divider circuit to be constructed of current mode logic components dependent upon particular environment of use to ensure optimum performance.

As to claim 11, it is seen as an obvious design choice for selecting phase control MUX to be constructed of current mode logic components dependent upon particular environment of use to ensure optimum performance.

Claims 21 and 22 recite similar limitations of claims 8-11. Therefore, they are rejected for the same reasons.

Response to Arguments

4. Applicant's arguments have been fully considered but they are not persuasive. In response to the arguments from line 3 of page 7 to line 7 of page 8. Ghoshal fails to teach a frequency divider coupled to the output of the phase locked loop figure 2. However, Hsu teaches a frequency divider (/M) coupled to the output of phase locked loop for reducing the output frequency. Therefore, it would have been obvious to one having ordinary skill in the art to add a frequency divider (M divider) at the output Ghoshal's figure 2 for the purpose of generate a clock signal having a frequency lower than the High frequency clock (22). Ghoshal's figure 2 further teach using a loop filter (FILTER circuit in 76) to facilitate the output of multiphase signals (58-68).

In response to Applicant's argument of claims 9-11, the combination of prior art having similar structure as applicant's figures therefore, the combination circuit having the same operating function as applicant's figures.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
November 16, 2002


Terry D. Cunningham
Primary Examiner